

APPROVED O.G. FIG.

BY CLASS SUBCLASS

DRAFTSMAN

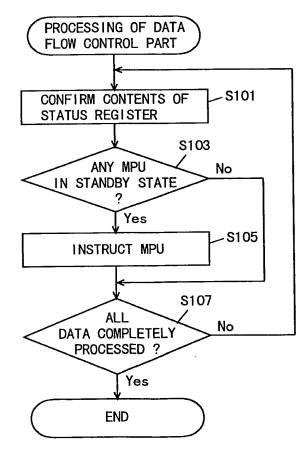
F I G. 2

EXEMPLARY STATUS REGISTER

	STANDBY	INPUT	PROCESSING	END OF PROCESSING	OUTPUT
MPU1	0	1	0	0	0
MPU2	1	0	0	0	0
MPU3	0	0	1	0	0
MPU4	0	0	0	0	1

FIG. 3

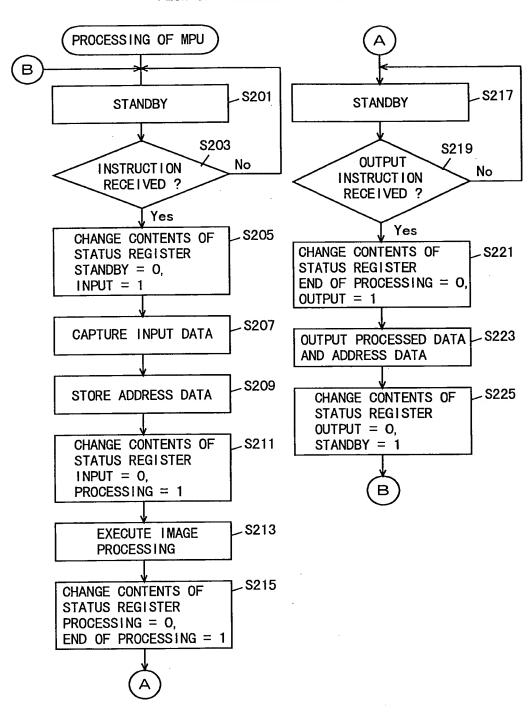
FLOW OF PROCESSING OF DATA FLOW CONTROL PART



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F I G. 4

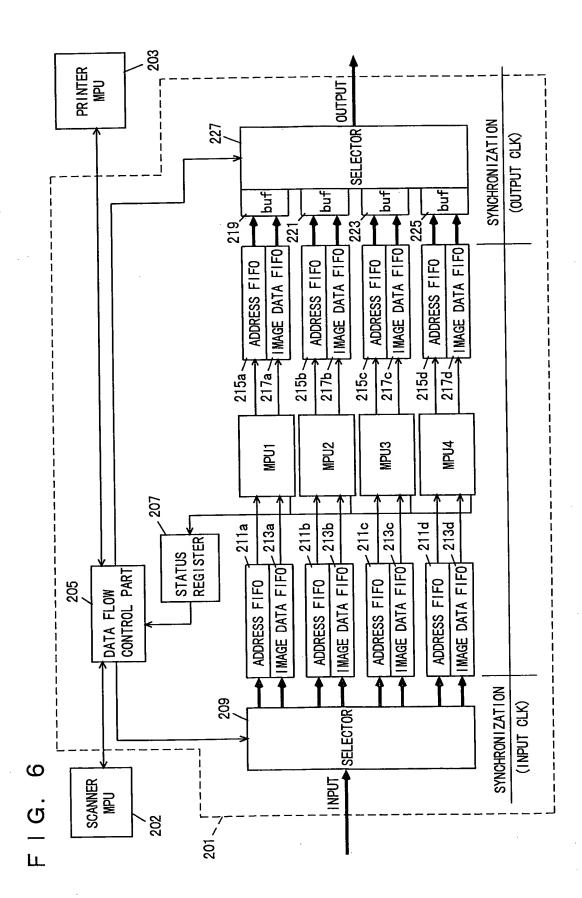
FLOW OF PROCESSING OF MPU



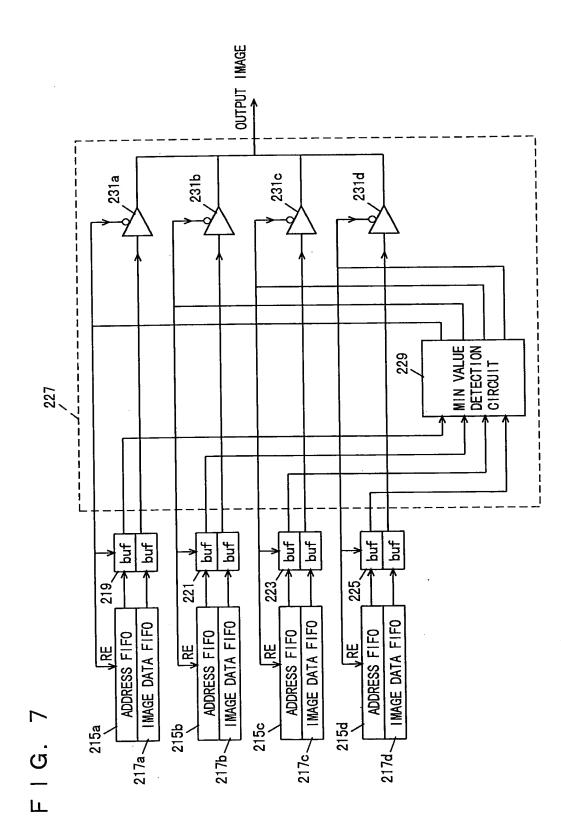
_

ES 쯆 A23 A20 A21 023 020 021 **B3** A30 සු 1331 D23 D21 **D**30 D 20 ន្ធ **K**2 8 A12 A13 A10 013 020 021 022 023 **D22 D13** 011 002 A11 A02 012 D10 110 010 011 012 OUTPUT DATA | Q01 | Q03 | Q00 ADDRESS DATA | A01 | A03 | A00 **D**02 8 83 8 \sqsubseteq 8 MPU2 MPU3 MPU4 퉏 8 Ŋ INPUT DATA D00 D01 т — Ω

DOWSKELY 111299



DOTENTAL THERE

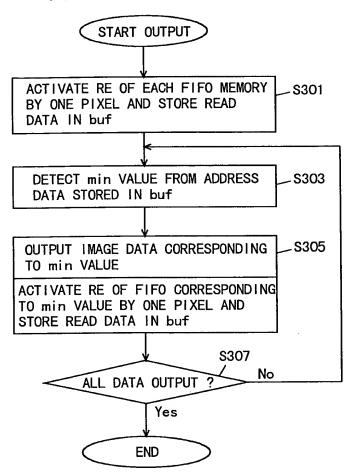


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APPHOVED	O.G. FIG.		
BY	CLASS	SUBCLASS	
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F I G. 8

OPERATION OF SELECTOR 227



F I G. 9

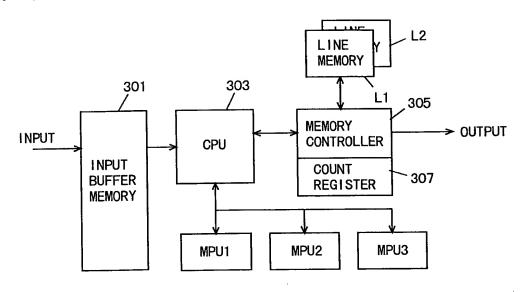
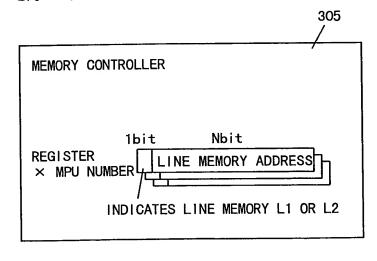


FIG. 10



APPROVED

FIG. 11

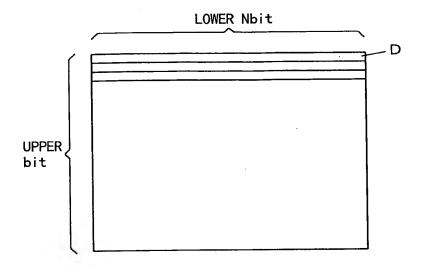


FIG. 12

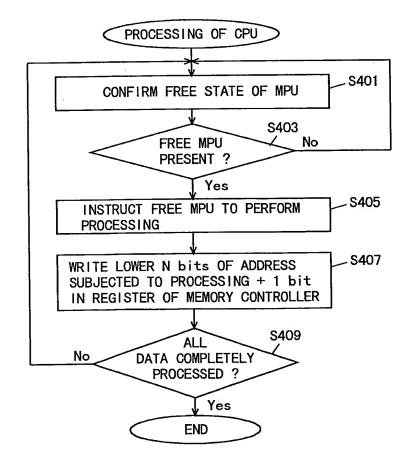


FIG. 13

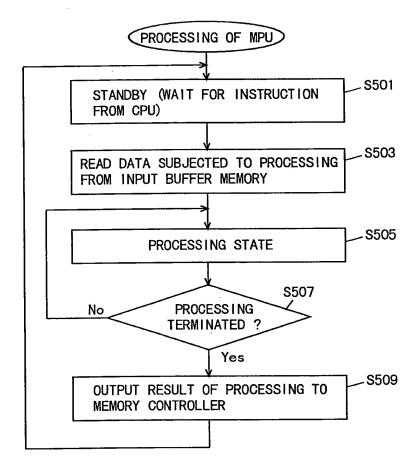
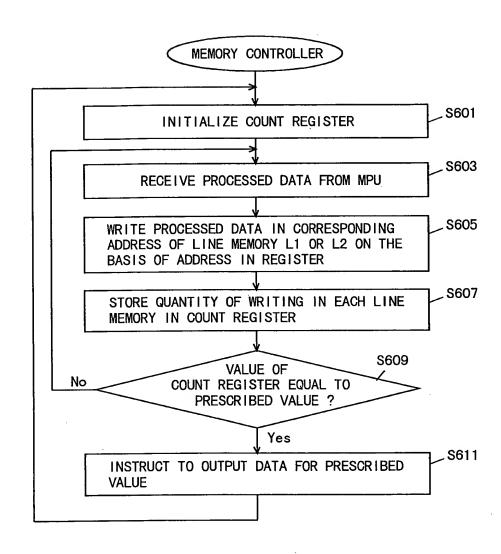


FIG. 14



COULTE ZASELOO

FIG. 15

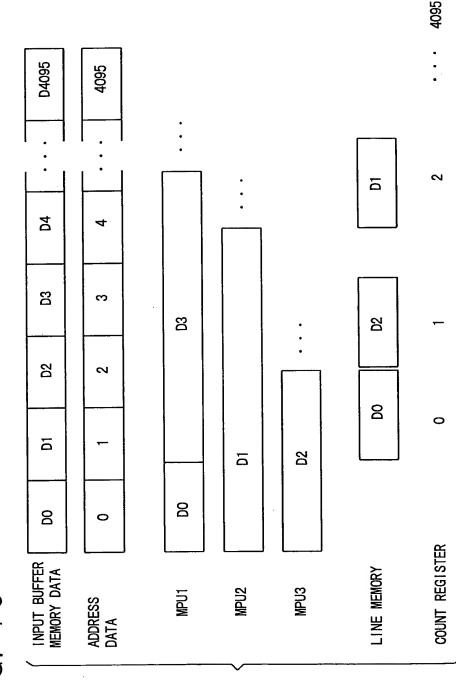


FIG. 16

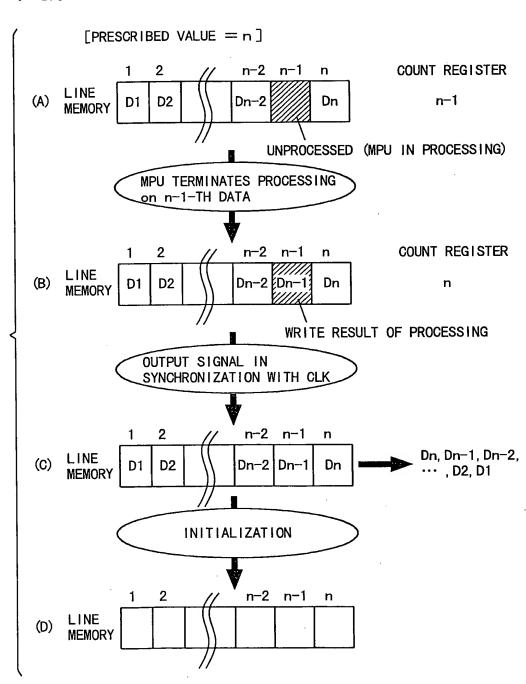


FIG. 17

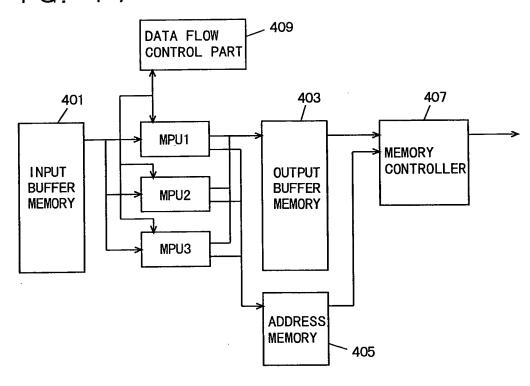


FIG. 18

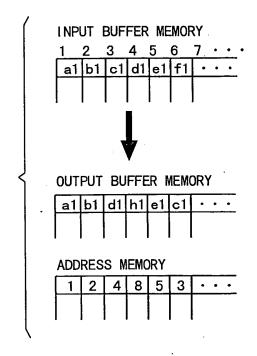


FIG. 19

[DATA FLOW CONTROL PART]

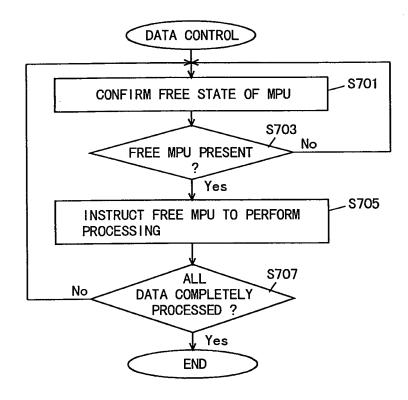


FIG. 20

[FLOW OF PROCESSING OF MPU]

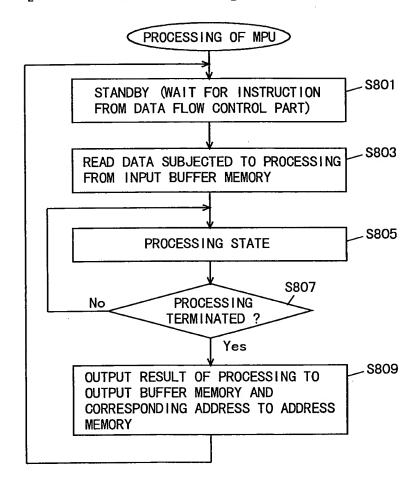


FIG. 21

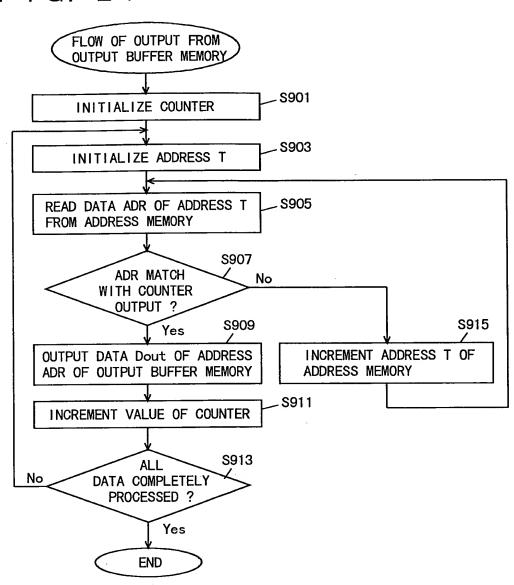
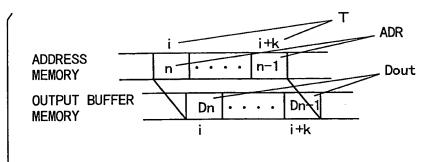


FIG. 22



SEARCH ADDRESS MEMORY FOR n-1

OUTPUT DATA Dn-1 OF ADDRESS i+k OF n-1 FROM OUTPUT BUFFER MEMORY

SEARCH ADDRESS MEMORY FOR n

OUTPUT DATA Dn OF ADDRESS i OF n FROM OUTPUT BUFFER MEMORY

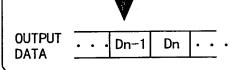
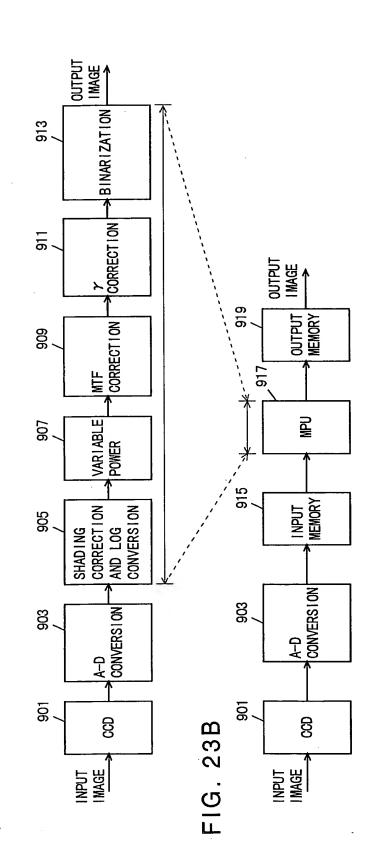


FIG. 25

L1 	L2 	L3 ↓	L4 ↓ _
D00	D01	D02	D03
D10	D11	D12	D13
D20	D21	D22	D23
D30	D31	D32	D33
D40	D41	D42	D43
D50	D51	D52	D53

FIG. 23A



APPROVĒD_	O.G. FIG.		
BY	CLASS	SUBCLASS	
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MPU4 MPU3 , 951 FEEDBACK FRAME MEMORY MPU₂ MPU1 952 STATUS REGISTER OUTPUT IMAGE BUS INPUT IMAGE BUS DATA FLOW CONTROL PART FEEDBACK BUS 953 7

F | G. 24



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